Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	394	duty adj cycle adj correction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 09:32
L2	306	1 and clock adj signals	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 09:33
L3	7	2 and control adj circuit and detect$3 and process adj variation and rates	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 09:38
L4	14	2 and control and detect$3 and process adj variation and rates	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 09:38
L5	7	4 not 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 09:39

phase with the input reference clock signal, and a second output clock signal (the quadrature or "Q" output clock signal) is 90 degrees out of phase with the input reference clock signal. Both output clock signals of the quadrature clock generator have the reference frequency. The output clock signals are phase mixed to provide a desired phase difference or delay between the output clock signal of the DLL and the input reference clock.

Brief Summary Text - BSTX (5):
Cyclic variations from the desired phase difference between the output clock signals of the quadrature clock generator result in "jitter." For DLL purposes, the jitter of the quadrature clock generator affects the timing margins of the DLL, increasing lock acquisition time for the DLL. Therefore, reduced jitter is desirable.

Brief Summary Text - BSTX (6):
According to one prior art method, a quadrature clock generator first divides the frequency of the input reference clock signal by two and then operates on the reduced frequency signal to produce two clock signals that are 90 degrees out of phase with one another. A DLL using a frequency dividing quadrature clock generator then must double the frequency of the clock signals to produce the desired output clock signals of the original frequency.

Brief Summary Text - BSTX (7):
According to an alternative prior art method, a quadrature clock generator operates "at frequency" to provide quadrature clock signals without the intermediate steps of frequency dividing and doubling. A fixed delay element is typically used to provide the desired phase relationship. When compared to frequency dividing quadrature clock generators, at frequency quadrature clock generators have the advantages of reduced circuit complexity, reduced die area, and reduced power consumption.

Brief Summary Text - BSTX (8):
Generally, frequency dividing quadrature clock generators are able to maintain the desired phase relationship between the output clock signals over a wider range of input reference clock frequencies than at frequency quadrature clock generators. Furthermore, when compared to at frequency quadrature clock generators, frequency dividing quadrature clock generators are better able to maintain the desired phase relationship in view of process variations, supply variations, and temperature variations.

Brief Summary Text - BSTX (12):
These and other objects are provided by a quadrature clock generator that includes an at frequency phase shifting circuit for providing the Q output clock signal and a first comparator for providing the I output clock signal. Both the phase shifting circuit and the second comparator are coupled to receive an input reference clock signal. The phase shifting circuit comprises a triangle wave generator coupled in series with a second comparator. The

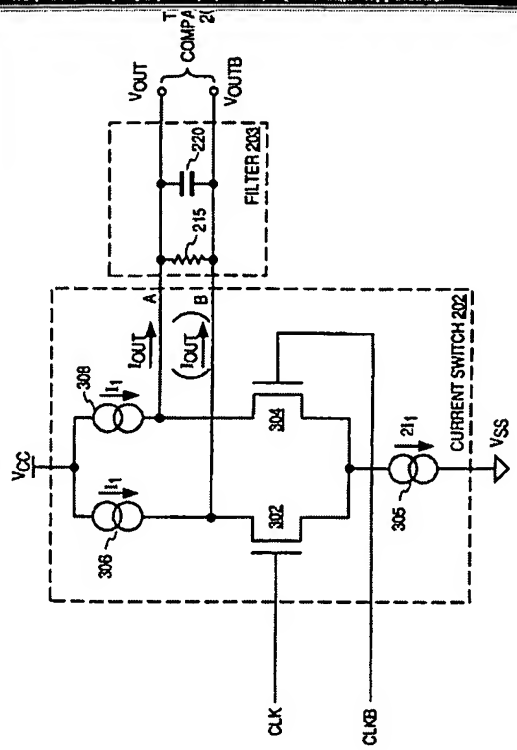

FIG. 3

US-PAT-NO: 6643790

DOCUMENT-IDENTIFIER: US 6643790 B1

TITLE: Duty cycle correction circuit with frequency-dependent bias generator

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Abstract Text - ABTX (1):

A duty cycle correction circuit operates by alternately speeding and slowing successive transitions of an input clock signal. By altering the rising and falling edge rates of a clock signal asymmetrically, the duty cycle of the clock signal is adjusted without shifting the DC level of the clock signal. In one embodiment, the duty cycle correction circuit includes current sources in place of resistive loads to avoid shifting the DC level of output clock signals. Frequency-dependent current sources that generate increased bias currents at higher frequency are used to achieve duty cycle correction over a broad range of input frequencies.

TITLE - TI (1):

Duty cycle correction circuit with frequency-dependent bias generator

Brief Summary Text - BSTX (4):

In many electronic circuit applications, it is desirable to generate a clock signal having a duty cycle as near to 50% as possible. For example, in chip-to-chip signaling applications in which data is transmitted or received on both rising and falling edges of a clock, it is important that successive rising and falling edges of the clock signal are evenly spaced in time. Otherwise, setup and hold requirements of signaling components may be not be met during the shorter half-cycle. Applications that employ delay-locked loop (DLL) circuits are also sensitive to uneven spacing between successive rising and falling clock signal edges, particularly when they include mixing circuitry operating at the same frequency as the reference clock. In that case, uneven spacing between successive rising and falling edges of the incoming clock signal usually results in unequal spacing in the phase offsets of the mixer output signals, degrading the delay locking performance of the circuit.

Brief Summary Text - BSTX (5):

FIGS. 1A, 1B and 1C illustrate a prior art duty cycle correction circuit 12 and corresponding input and output clock waveforms. The duty cycle correction circuit 12, referred to herein as a level-shifting corrector, receives an input clock signal (ICLK) and its complement (ICLK.backslash.) at respective inputs of a differential amplifier pair 14A, 14B. The differential pair 14A, 14B is biased by a current I sub 1 drawn by a constant current source 15. The drain

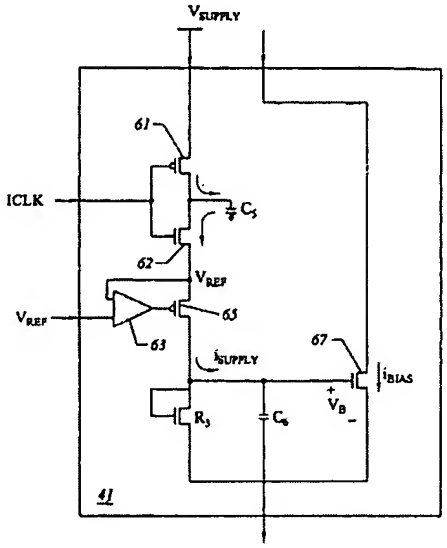

FIG. 3A

US-PAT-NO: 5614855

DOCUMENT-IDENTIFIER: US 5614855 A

TITLE: Delay-locked loop

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Abstract Text - ABTX (1):

A delay locked loop (DLL) is described in which a phase detector compares the phase of the output of the DLL with that of a reference input. The output of the phase comparator drives a differential charge pump which functions to integrate the phase comparator output signal over time. The charge pump output controls a phase shifter with unlimited range that adjusts the phase of the DLL output so that the output of the phase comparator is high 50% of the time on average. Because the DLL adjusts the phase shifter until the output of the phase detector is high 50% of the time, on average, the relationship of the DLL output clock to the input reference clock depends only on the type of phase detector used. For example, when a data receiver is used as the phase detector in the DLL, the output of the DLL is a clock signal which can be used as a sampling clock for data receivers elsewhere in the system, and is timed to sample data at the optional instant independent of temperature, supply voltage and process variations. Alternatively, a quadrature phase detector may be employed to generate a clock signal that possesses a quadrature (90.degree.) relationship with a reference clock signal input. This may be used, for example, to generate a transmit clock for a data transmission device. Furthermore, the DLL is controlled to minimize dither jitter while minimizing acquisition time. In addition, duty cycle correcting amplifiers are employed to produce a DLL output clock that has a desired duty cycle, for example 50%. Additionally, the inputs to the charge pump are reversed in alternate quadrants of the phase plane in order to enable unlimited phase shift with a finite control voltage range.

Brief Summary Text - BSTX (3):

The present invention relates to a circuit to generate periodic signals such as clock signals. More particularly, the present invention relates to a delay locked loop.

Brief Summary Text - BSTX (5):

Many high speed electrical systems possess critical timing requirements which dictate the need to generate a periodic clock wave form that possesses a precise time relationship with respect to some reference signal. Conventionally, a phase locked loop (PLL) which employs a voltage control oscillator (VCO) is used to provide the desired clock signal. An example of a PLL is shown in FIG. 1a. However, VCO-based PLLs have some undesirable

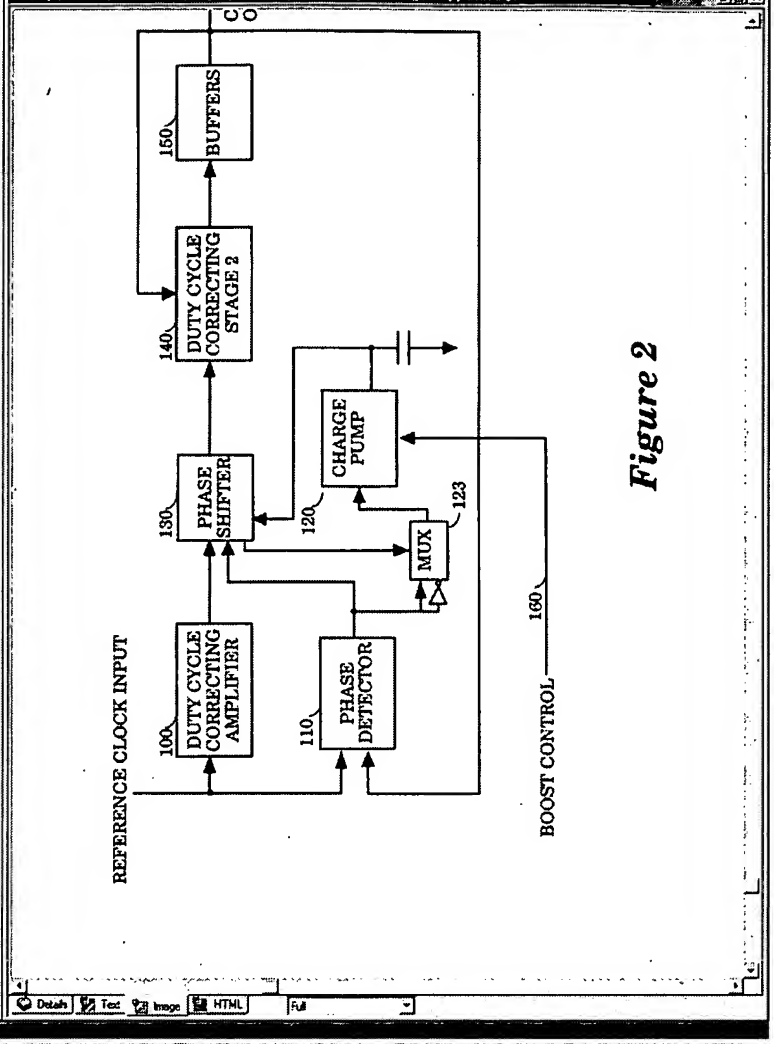

Figure 2